AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) An apparatus that facilitates self-correcting memory in a shared-memory system, comprising:

a main memory;

a memory controller coupled to the main memory;

a processor cache;

a communication channel coupled to the processor cache and to the memory controller; and

an error detection and correction mechanism within the memory controller, which is configured to cycle through and correct errors in main memory;

wherein after examining the data in ~~and possibly correcting~~ a location in main memory and correcting any errors, if the error detection and correction mechanism determines that the data from the location has been checked out to the processor cache, the error detection and correction mechanism is configured to read ~~and possibly correct~~ the corresponding line in the processor cache and correct any errors.

2. (Original) The apparatus of claim 1, wherein the error detection and correction mechanism performs single bit error correction/double bit error detection.

3. (Original) The apparatus of claim 1, wherein the error detection and correction mechanism performs double bit error correction.

4. (Original) The apparatus of claim 1, further comprising:

an input/output cache; and

wherein the reading mechanism is further configured to read the data from the input/output cache when the currently valid copy of the data is checked out to the input/output cache;

wherein the error detection and correction mechanism corrects errors in the data and stores the corrected copy of the data in the main memory.

5. (Original) The apparatus of claim 4, further comprising:

a second processor cache;

wherein the reading mechanism is further configured to read the data from the second processor cache when the currently valid copy of the data is checked out to the second processor cache; and

wherein the error detection and correction mechanism corrects errors in the data and stores the corrected copy of the data in the main memory.

6. (Original) The apparatus of claim 5, further comprising a marking mechanism within the memory controller that is configured to mark a location in the main memory to indicate that the data from the location is checked-out to a cache, wherein the cache is one of, the processor cache, the input/output cache, and the second processor cache.

7. (Original) The apparatus of claim 6, further comprising a scrubbing mechanism within the memory controller that is configured to access each

location within the main memory periodically to allow the error detection and correction mechanism to detect and correct errors.

8. (Original) The apparatus of claim 7, further comprising:

a detecting mechanism coupled to the scrubbing mechanism that is configured to detect the location in the main memory when the location is marked that the data from the location is checked-out to the cache; and

the reading mechanism that is further configured to request a read from the communication channel if the location is so marked.

9. (Original) The apparatus of claim 8, wherein the communication channel is a coherent network.

10. (Currently amended) A multiprocessor shared-memory computing system that facilitates self-correcting memory, comprising:

a main memory;

a memory controller coupled to the main memory;

a processor cache;

a central processing unit coupled to the processor cache;

a communication channel coupled to the processor cache and to the memory controller; and

an error detection and correction mechanism within the memory controller, which is configured to cycle through and correct errors in main memory;

wherein after examining the data in ~~and possibly correcting~~ a location in main memory and correcting any errors, if the error detection and correction mechanism determines that the data from the location has been checked out to the processor cache, the error detection and correction mechanism is configured to

read ~~and possibly correct~~ the corresponding line in the processor cache and correct any errors.

11. (Original) The multiprocessor shared-memory computing system of claim 10, wherein the error detection and correction mechanism performs single bit error correction/double bit error detection.

12. (Original) The multiprocessor shared-memory computing system of claim 10, wherein the error detection and correction mechanism performs double bit error correction.

13. (Original) The multiprocessor shared-memory computing system of claim 10, further comprising:

an input/output cache;

an input/output device coupled to the input/output cache; and

the reading mechanism further configured to read the data from the input/output cache when the currently valid copy of the data is checked out to the input/output cache;

wherein the error detection and correction mechanism corrects errors in the data and stores the corrected copy of the data in the main memory.

14. (Original) The multiprocessor shared-memory computing system of claim 13, further comprising:

a second processor cache;

a second central processing unit coupled to the second processor cache; and

the reading mechanism that is further configured to read the data from the second processor cache when the currently valid copy of the data is checked out to the second processor cache;

wherein the error detection and correction mechanism corrects errors in the data and stores the corrected copy of the data in the main memory..

15. (Original) The multiprocessor shared-memory computing system of claim 14, further comprising a marking mechanism within the memory controller that is configured to mark a location in the main memory to indicate that the data from the location is checked-out to a cache, wherein the cache is one of, the processor cache, the input/output cache, and the second processor cache.

16. (Original) The multiprocessor shared-memory computing system of claim 15, further comprising a scrubbing mechanism within the memory controller that is configured to access each location within the main memory periodically to allow the error detection and correction mechanism to detect and correct errors.

17. (Original) The multiprocessor shared-memory computing system of claim 16, further comprising:

a detecting mechanism coupled to the scrubbing mechanism that is configured to detect the location in the main memory when the location is marked that the data from the location is checked-out to the cache; and

the reading mechanism that is further configured to request a read from the communication channel if the location is so marked.

18. (Original) The multiprocessor shared-memory computing system of claim 17, wherein the communication channel is a coherent network.

19. (Currently amended) A method for facilitating self-correcting memory in a shared memory system, comprising:

marking as invalid a memory location within a plurality of memory locations when a data from the memory location is checked out to a cache;

scrubbing the plurality of memory locations for errors using an error detection and correction mechanism within the memory controller, which is configured to cycle through and correct errors in main memory;

detecting the memory location marked as invalid during scrubbing; and

upon detecting the memory location marked as invalid;

reading the data from the cache associated with the memory location,

correcting an error in the data, and

writing the data to the memory location.

20. (Original) The method of claim 19, wherein scrubbing the plurality of memory locations for errors includes:

accessing the memory location;

locating a valid copy of the data associated with the memory location;

reading the valid copy of the data;

correcting an error in the data;

writing the data to the memory location; and

repeating the steps of accessing, locating, reading, correcting, and writing for each memory location within the plurality of memory locations.